REMARKS

Amendments have been presented to claims 7, 16, and 33. These amendments were not done to overcome any of the cited articles and support for these changes are found throughout the specification.

35 U.S.C. 112, second paragraph, rejections

In the Office Action claims 16 and 33 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention.

The Examiner stated that the use of "selected" in claim 16 is unclear because the selecting is not positively recited. Although the Applicants believe that claim 16 was clear as previously presented, the Applicants have amended the claim to remove the "selected" reference.

Claim 33 has been amended to correct for a previously undetected drafting error.

The Applicants assert that amended claims 16 and 33 are in condition for allowance and respectfully request that the Examiner withdraw these rejections of these claims.

35 U.S.C. 102(b) rejection

In the Office Action claims 1-35 are rejected under 35 U.S.C. 102(b) as being anticipated by Chen. The Applicants traverse these rejections of these claims.

Claim 1, for example, reads:

> A data transfer block for use in an integrated circuit (IC) to interface an on-chip subsystem to an on-chip bus, the data transfer block comprising:
>
> a first and a second outbound queue to facilitate selective staging of a first and a second plurality of outbound bus transactions for the on-chip subsystem, at the choosing of the on-chip subsystem, each of said outbound bus transactions including a bus arbitration priority; and
>
> a first state machine coupled to the first and second outbound queues to service the first and second outbound queues, serially requesting for access to

the on-chip bus for the staged outbound bus transactions, according the first queue a first outbound priority and the second queue a second outbound priority, where access to the on-chip bus is granted to requesting bus transactions based at least in part on the included bus arbitration priorities of the contending bus transactions.

The Office Action states that this claim is anticipated by elements 322 and 326 of Fig. 14 and discussion at col. 17, lines 48-51 of Chen. The Applicants traverse this statement.

Chen does not teach, suggest, or discuss providing first and second outbound queues to stage outbound bus transactions of first and second outbound priorities, respectively. In Chen, the data queue 326 is the one and only queue of the arbitration node 44 to handle outbound responses. Nowhere does Chen mention a second outbound data queue, much less mention a state machine to accord a first queue a first outbound priority and a second queue a second outbound priority.

Even if one were to assume that Chen did teach a first and second outbound queues accorded a first and second outbound priorities, which the Applicants dispute, Chen still does not teach, suggest, or discuss that each of the outbound bus transactions will include a bus arbitration priority, as required by claim 1, for example. The data queue 326 in Chen is a simple first-in-first-out (FIFO) queue that bases priority on time of reception. There is nothing to suggest that the outbound bus transactions have an included bus arbitration priority, as required by claim 1, for example.

Additionally, Chen does not teach, suggest, or discuss an on-chip bus and an on-chip subsystem as described in claim 1, for example. First, the arbitration node of Chen is not coupled to a bus at all. The arbitration node 44 has dedicated ports that provide point-to-point connections between the arbitration nodes and the processor and I/O modules, see FIG. 13. Second, even if one were to argue that the arbitration node was coupled to a bus, which the Applicants dispute, there is nothing to suggest the bus would be on the same chip as the subsystem, as required by claim 1, for example.

Of course there may be other reasons why Chen does not anticipate claim 1; however, the Applicants believe that the above stated reasons are more than sufficient.

Therefore, the Applicants respectfully request that the Examiner withdraw this rejection claim 1.

Claims 2-6 depend from, and include the same limitations as, claim 1. Therefore, these claims are patentably distinct from Chen for at least the above reasons and the Applicants respectfully request that the Examiner withdraw these rejections of these claims.

Claim 7, for example, recites:

> A data transfer block for use in an integrated circuit (IC) to interface an on-chip subsystem to an on-chip bus, the data transfer block comprising:
>
> a first and a second inbound queue to facilitate selective staging of a first and a second plurality of inbound bus transactions for the on-chip subsystem, at the choosing of originating subsystems of the inbound bus transactions, each of the inbound bus transactions including a bus arbitration priority and being granted access to the on-chip bus based at least in part on the included bus arbitration priority; and
>
> a state machine coupled to the first and second inbound queues to service the first and second inbound queues, serially bringing the staged inbound bus transactions to the attention of the on-chip subsystem, according the first inbound queue a first inbound priority and the second inbound queue a second inbound priority.

The Office Action states that this claim is anticipated by elements 44 and 352 of Fig. 19a of Chen. The Applicants traverse this statement.

Chen does not teach, suggest, or discuss a first inbound queue and a second inbound queue to facilitate selective staging of transactions from an on-chip bus to an on-chip subsystem, as required by claim 7, for example. In Chen the input/output queues 352 connect the memory remote cluster adapter (MRCA) with external node remote cluster adapters (NRCAs). First, the I/O queues 352 are found on dedicated lines that provide point-to-point access between the arbitration node of the MRCA and the respective external NRCA. They do not stage inbound transactions from a bus. Second, even if one were to argue that they did stage inbound transactions for a bus, which the Applicants dispute, they still do not stage inbound transactions for an <u>on-chip</u> bus, as required by claim 7, for example. The I/O queues 352 facilitate communication

between the MRCA and external NRCAs of other clusters, see Chen column 10, lines 22-28.

Even if one were to assume that Chen had queues to facilitate selective staging of transactions from an on-chip bus to an on-chip subsystem, which the Applicants dispute, Chen still does not teach, suggest, or discuss according the first inbound queue a first inbound priority and the second inbound queue a second inbound priority, as required by claim 7, for example. The I/O queues 352, like all of the queues in Chen, are FIFO based queues and have no priority distinction amongst one another.

Of course there may be other reasons why Chen does not anticipate claim 7; however, the Applicants believe that the above stated reasons are more than sufficient. Therefore, the Applicants respectfully request that the Examiner withdraw this rejection claim 7.

Claims 8-9 depend from, and include the same limitations as, claim 7 and are therefore patentably distinct from Chen for at least the same reasons as claim 7. The Applicants respectfully request that the Examiner withdraw these rejection of these claims.

Claims 10-16 include limitations similar to at least some of the limitations discussed above. For example, these claims include limitations directed to an on-chip bus; a first and second outbound queues; and outbound bus transactions with bus arbitratration priorities. Because Chen does not teach, suggest, or discuss these limitations, these claims are patenable for at least these reasons. Therefore, the Applicants respectfully request the Examiner withdraw these rejections of these claims.

Claims 17-20 include limitations similar to at least some of the limitations discussed above. For example, these claims include limitations directed to a first and second inbound queues to facilitate staging of inbound transactions between and on-chip bus and an on-chip subsystem. Because Chen does not teach, suggest, or discuss these limitations, these claims are patenable for at least these reasons. Therefore, the Applicants respectfully request the Examiner withdraw these rejections of these claims.

Claim 21, for example, recites:

In a subsystem of an integrated circuit, a method of operation comprising:
determining intra-subsystem priorities for transactions with others subsystems of the integrated circuit to be serviced for requesting access to an on-chip bus of the integrated circuit, to which the subsystems are coupled;
generating and staging the transactions in accordance with the determined intra-subsystem priorities, including with each of the staged transactions a bus arbitration priority for use to arbitrate for access to the on-chip bus with other inter-subsystem transactions of other subsystems of the integrated circuit; and
serially servicing the staged transactions in accordance with their intra-subsystem priorities, requesting access to the on-chip bus for each staged transaction being serviced using the included bus arbitration priority.

As discussed above, Chen does not teach, suggest, or discuss an on-chip bus as required by claim 21, for example. Additionally Chen does not include any reference to subsystems of an integrated circuit. Chen teaches that many components may be in a single cluster 40; however, there is no suggestion that any of the components reside on the same chip. That is, Chen does not teach, suggest or discuss multiple subsystems of an integrated circuit, much less the communication between such subsystems described in claim 21.

Of course there may be other reasons why Chen does not anticipate claim 21; however, the Applicants believe the above stated reasons are more than sufficient. Therefore, the Applicants respectfully request that the Examiner withdraw this rejection of this claim.

Claims 22-24 depend from, and include the same limitations as, claim 21 and are therefore patentably distinct from Chen for at least the same reasons. The Applicants respectfully request that the Examiner withdraw these rejections of these claims.

Claims 25-26 include limitations similar to at least some of the limitations discussed above. For example, these claims include limitations directed to transactions having bus arbitration priorities and an on-chip bus. Because Chen does not teach, suggest, or discuss these limitations, these claims are patenable for at least these reasons.

Claim 27, for example, recites:

An integrated circuit comprising:
an on-chip bus; and
a plurality of subsystems coupled to the on-chip bus and interact with each other through transactions conducted across said on-chip bus, with each of the subsystems having a data transfer interface that interfaces the subsystem to the on-chip bus, and at least one of the data transfer interfaces allows the particular subsystem to initiate transactions with other subsystems in a prioritized manner, including a first intra-subsystem prioritization on the order transactions contending for the service of the at least one of the data transfer interfaces are to be serviced, and a second inter-subsystem prioritization on the order transactions of the various subsystems contending for the on-chip bus are to be granted access to the on-chip bus.

The Office Action states that the claim is anticipated by elements of Fig. 19b of Chen. The Applicants traverse this statement.

As discussed above, Chen does not teach, suggest, or discuss an on-chip bus as required by claim 27, for example. Additionally, Chen does not include a subsystem coupled to the on-chip bus through a data transfer interface to initiate transactions with other subsystems (also coupled to the on-chip bus) in a prioritized manner. The NRCA of Chen simply receives requests from internal arbitration nodes into respective queues. These requests are then granted access to the XBAR 362 in the order they are received. None of the internal arbitration nodes can send their request in a prioritized manner to bypass the default FIFO queuing order of the NRCA.

Claims 28-31 depend from, and include the same limitations as, claim 27 and are therefore patentably distinct from Chen for at least the same reasons. The Applicants respectfully request that the Examiner withdraw these rejections of these claims.

Claims 32-35 include limitations similar to at least some of the limitations discussed above. For example, these claims include limitations directed to an on-chip bus and transactions having bus arbitration priorities. Because Chen does not teach, suggest, or discuss these limitations, these claims are patenable for at least these reasons. Therefore, the Applicants respectfully request the Examiner withdraw these rejections of these claims.

CONCLUSION

In view of the foregoing, the Applicant respectfully submits that claims 1-35 are in condition for allowance. Thus, early issuance of Notice of Allowance is respectfully requested.

If the Examiner has any questions, he is invited to contact the undersigned at (503) 796-2972.

The Commissioner is hereby authorized to charge shortages or credit overpayments to Deposit Account No. 500393. A Fee Transmittal is enclosed in duplicate for fee processing purposes.

Respectfully submitted,
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